**Fault Isolation Engineer at Intel in Portland, Oregon**

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**Description**

**Job Description:**As a Fault Isolation Engineer you will be part of our Technology Development and Manufacturing Labs responsible for locating yield and reliability limiting failures on SRAM test vehicles and leading product chips for Intel's next generation Silicon, Assembly or Test Process Development and Manufacturing. The candidate must work in concert with Integration, Yield, Device and Quality & Reliability Engineers to enable robust failure rate models and risk assessments of the silicon/assembly processes under development to improve process performance, product yield, quality and/or reliability. The scope may include wafer and unit level Front-end Module, Back-End/Far Back-End Modules, Package Assembly, or Environmental Stress/Test capability.  
  
Your responsibilities will include but are not be limited to:  
  
o Utilizing modern techniques in fault isolation such as high-speed functional testers, IREM, LADA, nano-probing and TIVA to locate circuit fails quickly and reliably  
o Developing new test patterns and test methodologies for fault Isolation on future products  
o Authoring failure analysis reports and identifying root causes.  
o Supporting new process/product transfer and startup and the automation and improvement of the failure analysis process.  
o Collaborating with integration, device, and yield Engineers to assist in risk assessments.

**Qualifications**You must possess the below minimum qualifications to be consider for this position. Preferred qualifications are in addition to the minimum qualifications and are considered a plus factor in identifying top candidates. Experience can be obtained through a combination of prior education, current M.S./Ph.D. course work, projects, research and any relevant prior job/internships.  
  
**Minimum Qualifications:**  
o A technical college graduate with a M.S. or Ph.D. degree in Physics or Electrical Engineering within the last 18 months at time of hire.  
o Demonstrated strong knowledge of device physics, digital/analog circuit, and DFT architecture.   
o Knowledge of semiconductor fabrication, test and/or assembly packaging processing and associated materials.  
  
**Preferred Qualifications:**  
o Prior Intel Intern or Scholarship recipient  
o 1 year hands-on experience with lab equipment, including microscopy tools, such as SEM, DIB, TEM, AFM, nano-prober, oscilloscopes, or semiconductor parameter analyzers  
o Semiconductor device fabrication and characterization knowledge and experience  
o Knowledge and experience in functional testers, IREM, LADA, or TIVA are plus

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